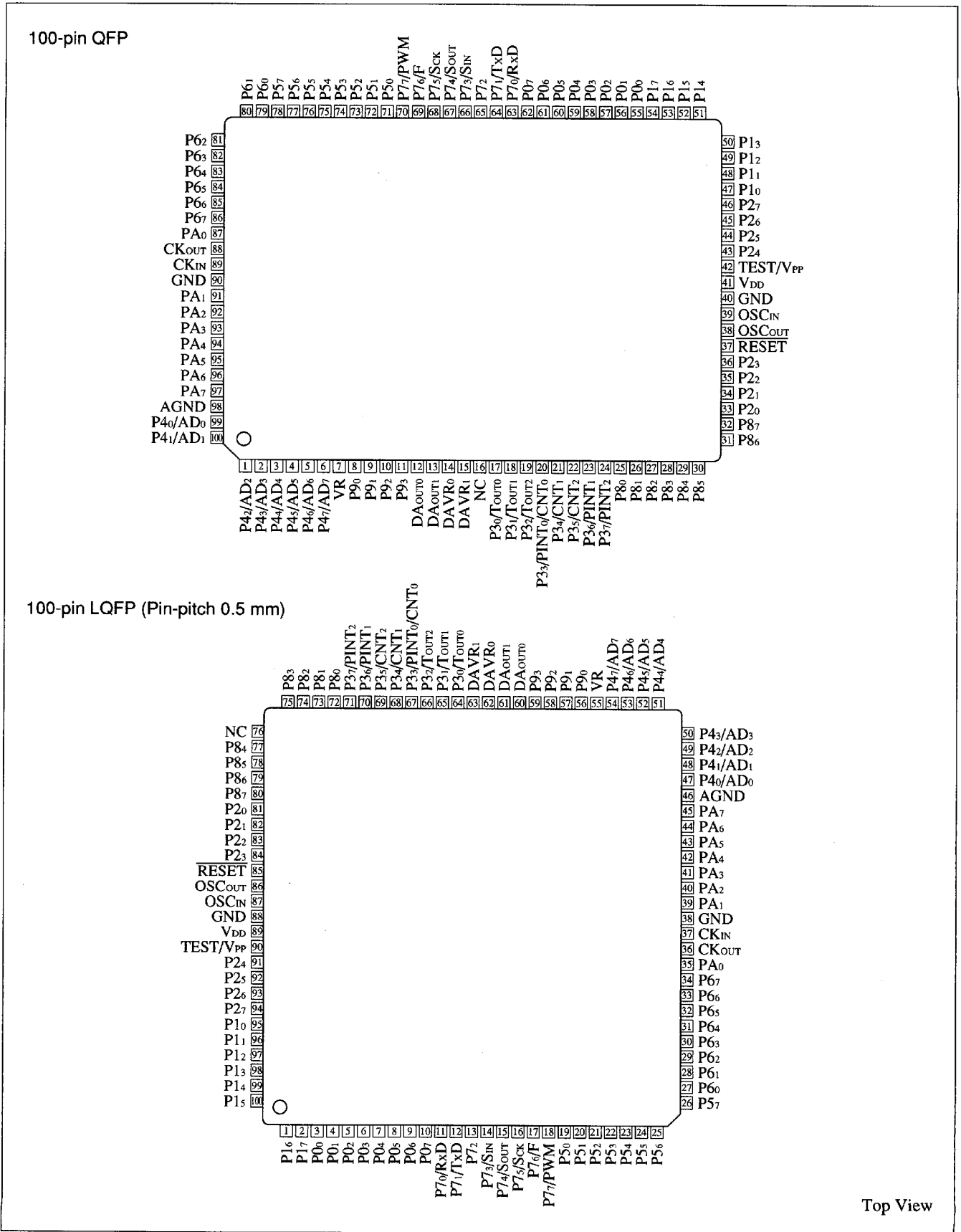


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| <p>10. I/O ports</p> <ul style="list-style-type: none"> • 2 input ports (each 8 bits) (one port also serves as A/D input) The pull-up resistor of one port can be turned on/off by software. • 2 output ports (each 8 bits) These are large current output pins. • 8-bit × 6 I/O ports and 4-bit × 1 I/O port The pull-up resistors can be turned on/off by software. <p>11. Timer/event counter</p> <ul style="list-style-type: none"> • Timer/event counter 16-bit × 1, 8-bit × 5 • These timers can output PWM (period and duty cycle of 1 channel are variable, duty cycle of 3 • Watchdog timer 8-bit × 1 • Clock timer 8-bit × 1 <p>12. Serial interface</p> <ul style="list-style-type: none"> • SIO 8-bit clock sync. × 1 • UART 8-bit clock async. × 1 <p>13. A/D converter</p> <ul style="list-style-type: none"> • Resolution 10-bit • Channel 8 channels | <p>14. D/A converter</p> <ul style="list-style-type: none"> • Resolution 8-bit (4-bit for waveform generator) • Channel 2 channels <p>15. Waveform generator</p> <ul style="list-style-type: none"> • Internal waveform RAM 2 channels • User programmable 16 level waveforms • Combined with external circuit, DTMF waveform can be output. <p>16. Clock output</p> <ul style="list-style-type: none"> • P7₆/F pin can be used to drive a buzzer (timer 5 output) <p>17. Operation power and voltage</p> <ul style="list-style-type: none"> • 2.7 to 3.6 V : system clock frequency 3.0 MHz (MAX.) • 4.5 to 5.5 V : system clock frequency 6.0 MHz (MAX.) <p>The LU8500F0/F1 can operate at the max. 12 MHz main clock if the operating voltage is in the range (2.7 to 5.5 V). However, the main clock frequency must be divided to the system clock according to the operating voltage range.</p> <p>18. Package</p> <ul style="list-style-type: none"> • LU8500F0 100-pin QFP (QFP100-P-1420) • LU8500F1 100-pin LQFP (LQFP100-P-1414)
(Pin-pitch 0.5 mm) |
|--|--|

<Flash memory features >

- | | |
|--|---|
| <p>1. Writing method</p> <ul style="list-style-type: none"> • Using instruction : in the same way as used for SHARP 8 M bits flash memory "LH28F008SA" • Auto byte write : through the command user interface (CUI) • V_{pp} = 12 V (external) <p>2. Erasing method</p> <ul style="list-style-type: none"> • Auto block erase by CUI. <p>3. Block configuration</p> <ul style="list-style-type: none"> • 8 blocks (1 block by 4k bytes, 7 blocks by 8k bytes) • Each block can be cleared independently. | <p>4. Reliability</p> <ul style="list-style-type: none"> • Write/erase cycle : 100 <p>5. Three writing modes</p> <ul style="list-style-type: none"> • PROM mode Program can be stored/erased by using general purpose PROM writer. • Serial mode (on-board mode) Data can be read/written/erased from PC. • Copy mode When the dedicated copy board is used, data stored in PROM can be copied into the internal flash memory. |
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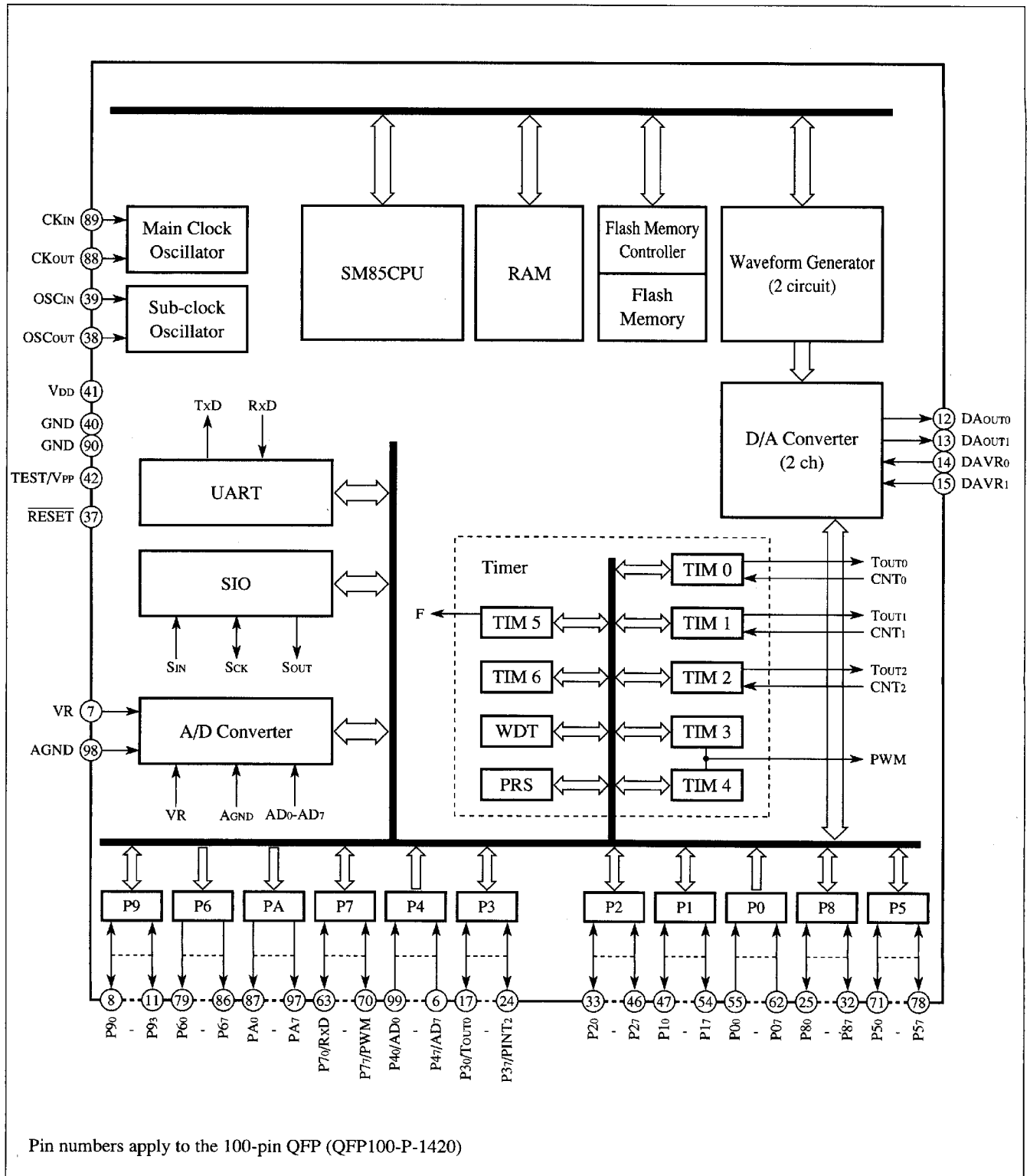
Pin Connections



Pin Description

Pin name	I/O	Function
P0 ₀ -P0 ₇	I	Input ports
P1 ₀ -P1 ₇	I/O	I/O ports / External memory data I/O ports
P2 ₀ -P2 ₇	I/O	I/O ports / External memory address output ports
P3 ₀ /TOUT ₀ -P3 ₂ /TOUT ₂	I/O	I/O ports / Timer outputs (TOUT ₀ , TOUT ₁ , TOUT ₂)
P3 ₃ /PINT ₀ /CNT ₀	I/O	I/O port / External interrupt input / Capture trigger input / Event count input (PINT ₀ /CNT ₀)
P3 ₄ /CNT ₁ , P3 ₅ /CNT ₂	I/O	I/O ports / Event count inputs (CNT ₁ /CNT ₂)
P3 ₆ /PINT ₁ , P3 ₇ /PINT ₂	I/O	I/O ports / External interrupt inputs (PINT ₁ /PINT ₂)
P4 ₀ /AD ₀ -P4 ₇ /AD ₇	I	Input ports / Analog input ports (AD ₀ -AD ₇)
P5 ₀ -P5 ₇	I/O	I/O ports / External memory address output ports
P6 ₀ -P6 ₇	O	Output ports (Large current output : 10 mA) (By mask option, the port can be configured as a N-ch open drain pin)
P7 ₀ /RxD	I/O	I/O port / UART data input
P7 ₁ /TxD	I/O	I/O port / UART data output
P7 ₂	I/O	I/O port
P7 ₃ /S _{IN}	I/O	I/O port / SIO data input
P7 ₄ /S _{OUT}	I/O	I/O port / SIO data output
P7 ₅ /S _{CK}	I/O	I/O port / SIO transfer clock I/O
P7 ₆ /F	I/O	I/O port (Buzzer output)
P7 ₇ /PWM	I/O	I/O port (PWM output)
P8 ₀ -P8 ₇	I/O	I/O ports
P9 ₀ -P9 ₃	I/O	I/O ports
PA ₀ -PA ₇	O	Output ports (Large current output : 10 mA) (By mask option, the port can be configured as a N-ch open drain pin)
DAVR ₀ , DAVR ₁	I	D/A converter reference voltage input ports
DAOUT ₀ , DAOUT ₁	O	D/A converter output ports
VR	I	A/D converter high-level reference voltage input port
AGND	I	A/D converter low-level reference voltage input port
CK _{IN} , CK _{OUT}	I, O	Oscillator pins for main clock (Connecting crystal oscillator)
OSC _{IN} , OSC _{OUT}	I, O	Oscillator pins for subclock (Connecting 32.768 kHz crystal oscillator)
RESET	I	Hardware reset signal input port
TEST/V _{PP}	I	Test pin (Connect to GND normally)/writing high voltage pin
V _{DD} , GND	I	Power supply pin, GND pin (Also serving as the D/A ground pin)

■ Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit	
Supply voltage	V_{DD}		-0.3 to +6.5	V	
Write voltage	V_{PP}		-0.2 to +14	V	
Input voltage	V_i		-0.3 to $V_{DD}+0.3$	V	
Output voltage	V_o		-0.3 to $V_{DD}+0.3$	V	
Maximum output current	High	I_{OH}	All output pins	4.0	mA
	Low	I_{OL1}	P60-P67, PA0-PA7	30	mA
		I_{OL2}	All output pin except P60-P67, PA0-PA7	4.0	mA
Total output current	High	ΣI_{OH}	All output pins	20	mA
	Low	ΣI_{OL1}	P60-P67, PA0-PA7	100	mA
		ΣI_{OL2}	All output pin except P60-P67, PA0-PA7	20	mA
Operating temperature	T_{opr}		-20 to +70	°C	
Store temperature	T_{stg}		-55 to +125	°C	

Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit	Note
Supply voltage	V_{DD}	at 3 V mode	2.7 to 3.6	V	
		at 5 V mode	4.5 to 5.5		
System clock cycle	t_{SYS}	$V_{DD}=4.5$ to 5.5 V	0.17 to 61	μ s	
		$V_{DD}=2.7$ to 3.6 V	0.33 to 61		
Maximum system clock frequency	f_{smax}	$V_{DD}=4.5$ to 5.5 V	6.0	MHz	
		$V_{DD}=2.7$ to 3.6 V	3.0		
Maximum main clock frequency	f_{main}	$V_{DD}=4.5$ to 5.5 V	12.0	MHz	1
		$V_{DD}=2.7$ to 3.6 V	6.0		
Subclock frequency	f_{sub}	$V_{DD}=2.7$ to 3.6 V	32.768	kHz	
		$V_{DD}=4.5$ to 5.5 V			
Operating temperature	t_{opr}		-20 to +70	°C	

Note 1. The system clock is divided-by-2 main clock. When deriving the system clock from a clock source other than divided-by-2 main clock, the main clock can be set to match the system clock frequency.

DC Electrical Characteristics

(V_{DD}=2.7 to 3.6 V, T_a=-20 to +70 °C)

Parameter	Symbol	Condition	Rating			Unit	Note
			MIN.	TYP.	MAX.		
Input voltage	V _{IH1}		0.8V _{DD}		V _{DD}	V	2
	V _{IL1}		0		0.2V _{DD}		
	V _{IH2}		V _{DD} -0.3		V _{DD}	V	3
	V _{IL2}		0		0.3		
Input current	I _{IH1}	V _{IN} =V _{DD} , V _{DD} =3.0 V			10	μA	4
	I _{IL1}	V _{IN} =0 V, V _{DD} =3.0 V			-10		
	I _{IL2}	V _{IN} =0 V, V _{DD} =3.0 V	-10	-25	-50	μA	5
Output voltage	V _{OH1}	I _{OH} =-0.6 mA, V _{DD} =3.0 V	V _{DD} -0.5			V	6
	V _{OL1}	I _{OL} =6.0 mA, V _{DD} =3.0 V			1.0		
	V _{OH2}	I _{OH} =-0.6 mA, V _{DD} =3.0 V	V _{DD} -0.5			V	7
	V _{OL2}	I _{OL} =0.6 mA, V _{DD} =3.0 V		0			
A/D conversion	Resolution			10		bits	
	Differential linear tolerance	VR = V _{DD} = 3.0 V f _{sys} = 3.0 MHz		±1.0	±2.5	LSB	
	Linear tolerance			±3.0	±5.0	LSB	
	Combined tolerance			±4.0	±6.0	LSB	
D/A conversion	Resolution		DAVR = V _{DD} = 3.0 V		8.0		bits
	Output voltage range	0.8			V _{DD} -0.8	kΩ	
	Total tolerance			±0.03	±0.06	V	
Current consumption	I _{DD}	f _{sys} = 3.0 MHz		9.0	15	mA	9
	I _{DDH}	f _{sys} = 3.0 MHz, HALT mode		1.0	2.0		
	I _{DDS1}	OSC running, STOP mode		20	40	μA	10
	I _{DDS2}	OSC in stop, STOP mode		1.0	6.0	μA	11

Note 2. Applied to pins P10-P17, P20-P27, P30-P32, P40-P47, P50-P57, P71, P72, P74, P76, P77, P80-P87, P90-P93, CKIN

Note 3. Applied to pins RESET, OSCIN, P00-P07, P33-P37, P70, P73, P75

Note 4. Applied to pins (with pull-up resistors disconnected) P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P70-P77, P80-P87, P90-P93

Note 5. Applied to pins RESET

(with pull-up resistors disconnected) P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P87, P90-P93

Note 6. Applied to pins P60-P67, PA0-PA7

Note 7. Applied to pins P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P87, P90-P93

P00 (RD), P01 (WR) (in external memory expansion mode)

Note 8. Applied to pins DAOUT0, DAOUT1

Note 9. Without load V_{DD}=3.0 V, main clock frequency = 16 MHz

Note 10. Without load V_{DD}=3.0 V, OSC running (32.768 kHz), VR=GND, constant input signal

Note 11. Without load V_{DD}=3.0 V, OSCIN=GND, VR=GND, constant input signal

($V_{DD}=4.5$ to 5.5 V, $T_a=-20$ to $+70$ °C)

Parameter	Symbol	Condition	Rating			Unit	Note
			MIN.	TYP.	MAX.		
Input voltage	V_{IH1}		$0.8V_{DD}$		V_{DD}	V	12
	V_{IL1}		0		$0.2V_{DD}$		
	V_{IH2}		$V_{DD}-0.5$		V_{DD}	V	13
	V_{IL2}		0		0.5		
Input current	I_{IH1}	$V_{IN}=V_{DD}, V_{DD}=5.0$ V			-10	μ A	14
	I_{IL1}	$V_{IN}=0$ V, $V_{DD}=5.0$ V			10		
	I_{IL2}	$V_{IN}=0$ V, $V_{DD}=5.0$ V	-40	-75	-150	μ A	15
Output voltage	V_{OH1}	$I_{OH}=-1.0$ mA, $V_{DD}=5.0$ V	$V_{DD}-0.5$			V	16
	V_{OL1}	$I_{OL}=10$ mA, $V_{DD}=5.0$ V			2.0		
	V_{OH2}	$I_{OH}=-1.0$ mA, $V_{DD}=5.0$ V	$V_{DD}-0.5$			V	17
	V_{OL2}	$I_{OL}=1.0$ mA, $V_{DD}=5.0$ V		0			
A/D conversion	Resolution			10		bits	
	Differential linear tolerance	$V_R=V_{DD}=5.0$ V $f_{sys}=6.0$ MHz		± 1.0	± 2.5	LSB	
	Linear tolerance			± 3.0	± 5.0	LSB	
	Combined tolerance			± 4.0	± 6.0	LSB	
D/A conversion	Resolution		$DAVR=V_{DD}=5.0$ V		8.0		bits
	Output voltage range	0.8			$V_{DD}-0.8$	k Ω	
	Total tolerance			± 0.05	± 0.10	V	
Current consumption	I_{DD}	$f_{sys}=6.0$ MHz		20	30	mA	19
	I_{DDH}	$f_{sys}=6.0$ MHz, HALTmode		3.0	6.0		
	I_{DDs1}	OSC running STOP mode		30	60	μ A	20
	I_{DDs2}	OSC in stop, STOP mode		1.0	10	μ A	21

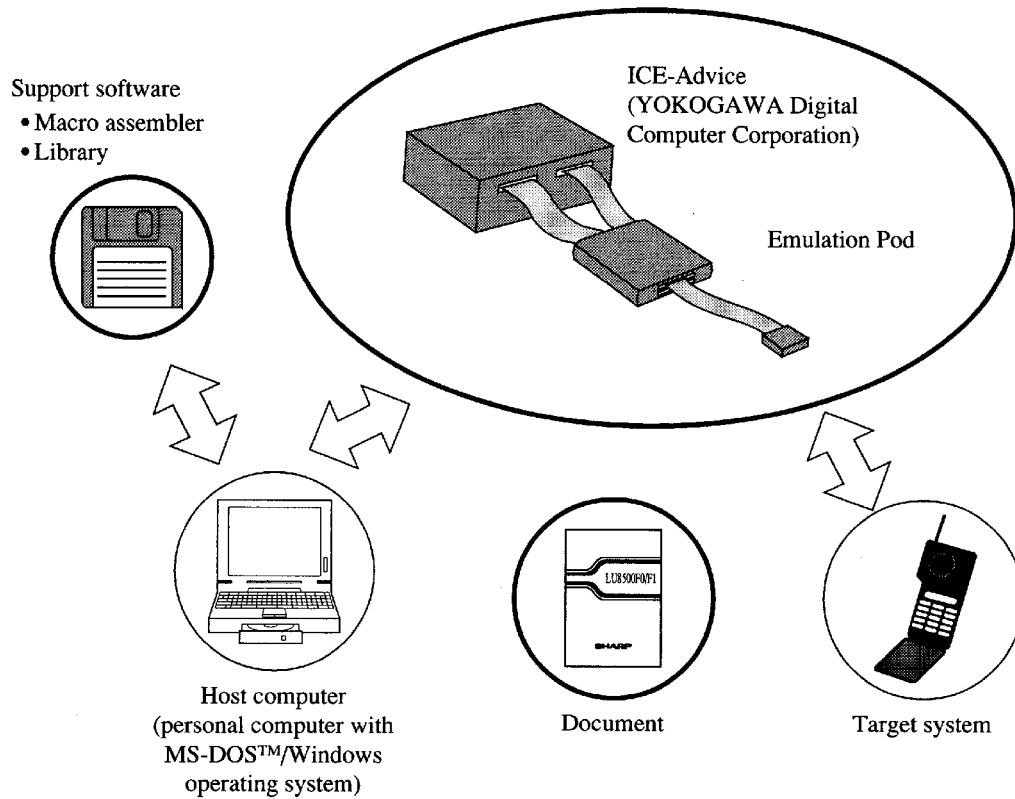
- Note 12. Applied to pins P10-P17, P20-P27, P30-P32, P40-P47, P50-P57, P71, P72, P74, P76, P77, P80-P87, P90-P93, CKIN
- Note 13. Applied to pins \overline{RESET} , OSCIN, P00-P07, P33-P37, P70, P73, P75
- Note 14. Applied to pins (with pull-up resistors disconnected) P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P70-P77, P80-P87, P90-P93
- Note 15. Applied to pins \overline{RESET}
(with pull-up resistors disconnected) P00-P07, P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P87, P90-P93
- Note 16. Applied to pins P60-P67, PA0-PA7
- Note 17. Applied to pins P10-P17, P20-P27, P30-P37, P50-P57, P70-P77, P80-P87, P90-P93
P00 (\overline{RD}), P01 (\overline{WR}) (in external memory expansion mode)
- Note 18. Applied to pins DAOUT0, DAOUT1
- Note 19. Without load $V_{DD}=5.0$ V, main clock frequency = 12 MHz
- Note 20. Without load $V_{DD}=5.0$ V, OSC running (32.768 kHz), $V_R=GND$, constant input signal
- Note 21. Without load $V_{DD}=5.0$ V, OSCIN=GND, $V_R=GND$, constant input signal

LU8500F0/F1 Development Support System

The software program for LU8500F0/F1 can be developed through a system consisting of a personal computer (MS-DOS™)* serving as a host, an in-circuit emulator and many types of development devices for user's system evaluation.

If a GP-IB interface is used in place of the standard RS-232C interface, programs can be transferred to an emulator at high speed.

* MS-DOS™ is a trademark of Microsoft Corporation.



ICE	Debugger	Support language
YOKOGAWA Digital Computer Corporation AD200-S56/PP150A	Micro VIEW-G (Windows)	<ul style="list-style-type: none"> • Assembler (SHARP) • Structured assembler / C compiler (ADaC Corporation)

SHARP

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- Office automation equipment
- Telecommunication equipment (except for trunk lines)
- Test and measurement equipment
- Industrial control
- Audio visual equipment
- Consumer electronics

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- Transportation control and safety equipment (i.e. aircraft, trains, automobiles, etc.)

- Traffic signals
- Gas leakage sensor breakers
- Alarm equipment
- Various safety devices, etc.

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- Telecommunication equipment (trunk lines)
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